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Design and Comparison of Encoder for Flash ADC Using Cadence Tool

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Abstract

Background / Objectives: The Design of encoder for Flash ADC using cadence virtuoso presents a encoder design for Flash ADCs, aiming to reduce Power consumption, increase speed and reduce the area and achieving resolution.
Methods / Statistical Analysis: The various encoder architecture like Multiplexer based direct conversion architecture Intermediate Gray code-based Encoder using basic gates, Wallace Tree Encoder and Gray code-based encoder using 2:1 Multiplexer employs to mitigate common challenges such as Thermal noise and Mismatches, Linearity and Area constraint.
Findings / Applications: Through extensive simulations and analyses, our design demonstrates improved performance metrics, including high speed and less Power consumption and Area.

Keywords: Power, Speed, Area.

1. Introduction

With the merit of the digital circuit that gives strong motivation to make the digital world, the main aspect in nature is that real world signals are analog signals. This naturally occurring signal is made to digital for accuracy and better quality. In this modern era of electronics portable devices and high-end instruments are becoming more and more sophisticated and perform a variety of tasks with high precision. The trend toward increased integration of analog and digital signals needs data converters such as ADC, DAC is embedded in large digital IC's. There are various architectures in ADC and selected depending on the application. One such relatively easy architecture which is used for converting continuous time varying signal to digital signal is Flash ADC. Flash ADCs are mainly used in high-speed applications and are known for its high-power consumption. In Flash ADC itself there are various blocks such as resistor ladder, Comparator array, Thermometer code to Binary code encoder etc. Even though the comparator array and resistor ladder consume the major part of ADC power, the encoder part also plays some significant role of ADC. The applications collectively underscore the versatility and significance of flash ADCs across diverse technological domains drives.

2. Literature Survey

Dr. George Tom Varghesea and Prof. Dr. Kamalakanta Mahapatra, was proposed by A 4-bit Flash Analog-to-Digital Converter (ADC) implemented with 180 nm CMOS technology utilizes an

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innovative design approach. Instead of conventional comparators, it employs inverter-based comparators to minimize silicon area and power consumption. Additionally, to enable operation at lower voltages, low threshold voltage MOSFETs are integrated [1].

Jyothi Kamatam, Kumaraswamy Gajula and Y.Aruna Suhasini, was A proposed pipelined 4-bit flash ADC, utilizing 0.18um CMOS technology, aims to achieve high speed while minimizing power consumption, conversion time, and silicon area. This design emphasizes a conservative physical layout, focusing on reducing analog circuitry to enhance performance, making it suitable for demanding high-speed ADC applications [2].

Rahul D.Marotkar and Dr. M. S. Nagmode, was praposed A 4-bit flash ADC employs an exceptionally efficient low-power encoder strategy, tailored for gigahertz operation. Implemented in 90nm technology with a 1.2V power supply, the encoder utilizes pseudo NMOS logic style to boost speed and minimize power consumption, while also mitigating bubble errors arising from test and hold circuitry and signal delays. Notably, the average power consumption is reduced to 0.3149mW, underscoring its energy-efficient design for high-speed applications [3].

S. Sheikhaei, S. Mirabbasi, A. Ivanov, "An Encoder for a 5GS/s 4bit flash A/D converter in 0.18um CMOS", In this paper a voltage to time converter is presented for use in time-based analog to digital converter. The converter runs with a 5GHz input clock [4].

S. Abdullah, Almansouri, Abdullah Alturki, Hossein Fariborzi, Khaled N. Salama and Talal Al-Attar "A 12.4fJ-FoM 4-bit flash ADC based on the strong-arm architecture." In this paper Proposed design eliminates the need for the resistive ladder by systematically modifying the sizing of input differential pair of each comparative [5].

3. Problem Statement

- Develop low power Flash ADC architecture capable of achieving resolution of least bits while minimizing energy consumption for battery operated application.
- Achieving a high resolution while maintaining a fast conversion speed is a significant challenge.
- The primary challenge in high-speed Flash ADC design lies in accurately converting the thermometer code to binary, as timing disparities between clock and input signals, along with inherent delays, often lead to bubble errors. To mitigate these errors effectively, leveraging majority logic of 0's and 1's proves beneficial.

4. Objectives

- In proposed design to minimize power dissipation, current dissipation and propagation delay using direct conversion of thermo-meter-code to binary code.
- To increase the speed of Flash ADC multiplexer based direct conversion method.
- To reduce the bubble errors while converting the thermometer code to Gray code, Intermediate Gray code-based encoder is used.

5. Flash ADC

As the number of bits increases in flash ADCs, the complexity escalates due to the requirement of a larger number of comparators, impacting both circuit area and power consumption. The main significance of flash ADC is that they are used within pipeline and sigma delta converters. The flash ADC consists of three main components resistor string, comparator bank, encoder logic. For N bit ADC, 2N resistors and 2N-1 comparators and 2N-1 to N bit encoder is needed. The block diagram for typical flash ADC architecture is shown below.

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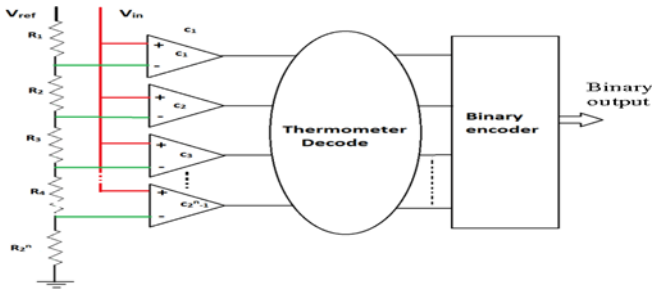

Figure 1. Flash ADC

6. Encoder Block

The thermometer code requires very huge memory since it takes a greater number of bits (2N -1) to represent digital equivalent of a sample. It will become very complex to process this code in further levels. Hence it is very crucial to convert thermometer code in to some other code that represents the equivalent data with optimized number of bits (N) like binary code. There are two types of encoders for conversion, known as

- Direct conversion of thermo-meter-code to binary code
- Indirect conversion of thermo-meter-code to binary code.

Multiplexer based direct conversion Architecture

In this architecture the thermometer code is directly converted to the binary code using 2:1multiplexers. From the truth table it is clear that the bit B4 is equivalent to the thermometer code T8. Then the bit B3 can be obtained from T12 and T4 by keeping T8 as select line for the Multiplexer. Similarly, all the bits are directly obtained from the input thermometer codes. This architecture is one of the most common architectures used in ADC design because of its low power consumption and high speed. For a 4-bit encoder it requires 11 2:1 multiplexer.

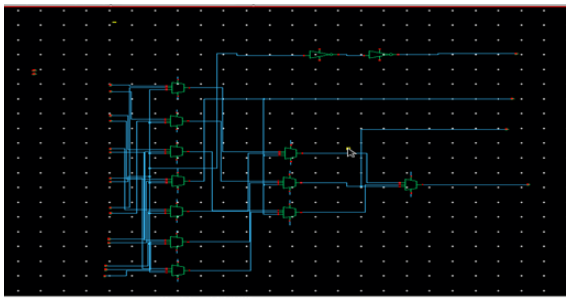

Figure 2. Schematic of Multiplexer Based Direct Architecture

Intermediate Gray code-based Architecture

In this architecture the thermometer code is directly converted to its corresponding Gray code and then it converted to binary. This technique is very highly power efficient in nature. Other than power efficiency, converting the thermometer code to Gray code will help in reducing the bubble errors. The conversion of Gray code to binary code is done using the basic logic gates (AND, OR and INVERTER) by the equations shown below:

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$$G_3 = T_8$$
$$G_2 = T_4\overline{T_{12}}$$
$$G_1 = T_2\overline{T_6} + T_{10}\overline{T_{14}}$$
$$G_0 = T_1\overline{T_3} + T_5\overline{T_7} + T_9\overline{T_{11}} + T_{13}\overline{T_{15}}$$

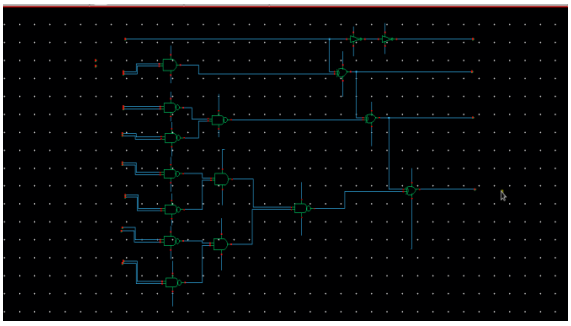

Figure 3. Schematic of Intermediate Gray Code Based Architecture

Wallace Tree Encoder

The inputs to the Wallace tree encoder are typically binary bits. Let's say you have n inputs. The inputs are grouped into sets of binary numbers. These groups are then processed in parallel. Usually, the inputs are divided into groups of three bits each. Within each group, the partial sums are then fed into a tree structure. The result of this final addition gives the binary encoding of the number of ones in the original input set. The output of the Wallace tree encoder is typically a binary number that encodes the number of ones in the input set. The advantage of the Wallace tree encoder is its parallelism, which allows it to process multiple bits simultaneously, making it efficient for hardware implementations where speed and efficiency are crucial.

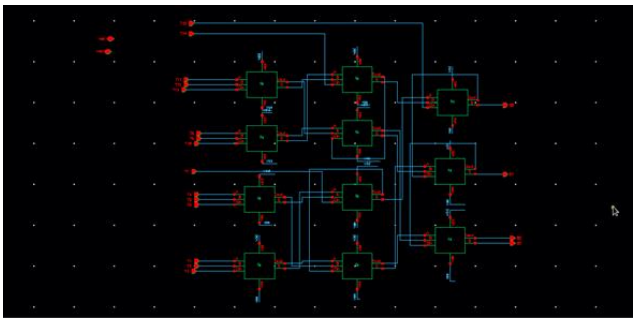

Figure 4. Schematic of Wallace Tree Encoder

Gray code-based Encoder Using 2:1 Multiplexer

Gray code based Transforming thermometer code to binary encoder for an ADC using 2:1 Multiplexers. This is the same logic reported in Intermediate Gray Code based Encoder. Here we have to use additional inverters at the input port to get the gray code. These extra inverters spoil the advantage of this architecture in terms of power consumption and area. Moreover, it requires 11 multiplexers for the realization of 4-bit architecture.

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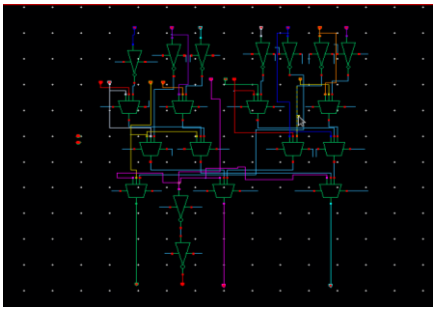

Figure 5. Schematic of Gray code-based Encoder Using 2:1 Multiplexer

7. Result

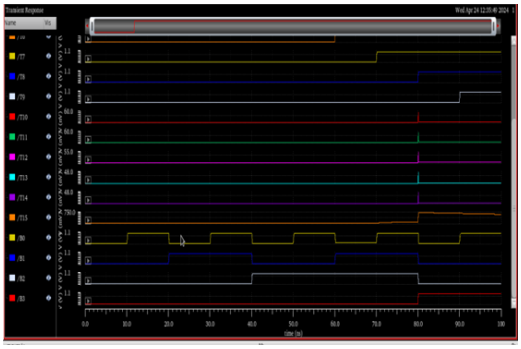

Figure 6. Transient Response of Multiplexer Based Direct Architecture

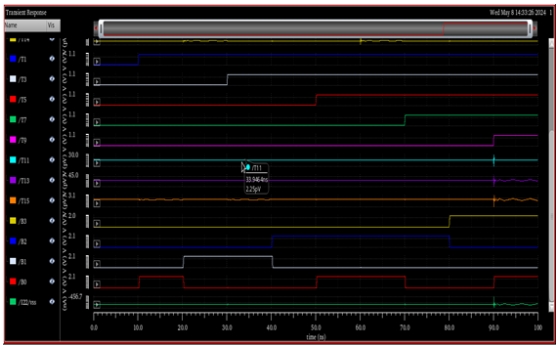

Figure 7. Transient Response of Intermediate Gray code-based Architecture

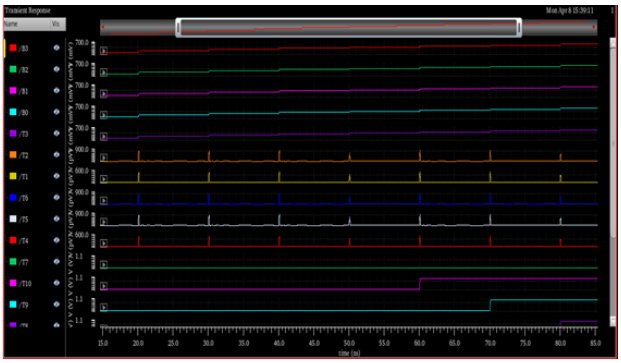

Figure 8. Transient Response Wallace Tree Encoder

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8. Comparison of Different Architecture

Table 1. Comparison

Architecture	Technology	Power Supply (V)	Power Consumption (µW)	Delay(ns)
Conventional Multiplexer Based Architecture	90nm	1.5	12.00	0.3730
Intermediate Gray code Based Architecture	90nm	1.5	11.08	0.5232
Wallace Tree Architecture	90nm	1.5	61.93	0.9663
Gray Code based Encoder	90nm	1.5	21.31	0.5299

9. Conclusion

Conventional Multiplexer based architecture have power consumption and delay of 12µW, 0.3037ns respectively. Intermediate Gray code-based architecture has power consumption and delay of 11.08µW, 05232ns respectively. Wallace tree code-based architecture have power consumption and delay of 61.93µW, 0.9663ns respectively. And Gray code-based architecture having the power consumption and delay of 21.31µW, 0.5299ns respectively.
Here we conclude that, Intermediate Gray code-based architecture consumes low power compared to other architecture. For high speed, Conventional Multiplexer based Architecture is preferred.

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